

IN THE CLAIMS

Please cancel Claim 1 without prejudice or disclaimer.

Claim 1 (cancelled).

Claim 2 (currently amended): A voltage regulator including a transistor (10), having a main current path between the input voltage terminal (V_{in}) of said voltage regulator and the output of said voltage regulator, comprising:

an amplifier (20) having an output being connected to the control terminal (16) of said transistor (10) and to the one input (22) of which a voltage as a function of the output voltage (V_{out}) of said voltage regulator is applied,

a transconductance amplifier (30) having a output being connected to the other input (24) of said amplifier (20),

a first resistor (R_{o1}),

a capacitor (C_c) wherein the one input (32) of said transconductance amplifier (30) is connected to a further voltage as a function of said output voltage (V_{out}) of said voltage regulator whilst the other input (34) of said transconductance amplifier (30) is connected to a reference voltage (V_{ref}) dictating said output voltage (V_{out}) of said voltage regulator, and

a further resistor (R_{sz}) is coupled between the one input (22) and the other input (24) of said amplifier (20),

~~The voltage regulator as set forth in Claim 1~~ wherein the value of said further resistor (R_{sz}) is selected to substantially maximize the phase reserve of said voltage regulator.

Claim 3 (currently amended): The voltage regulator as set forth in Claim 4 2 wherein said transistor (10) is a PMOS field-effect transistor.

Claim 4 (currently amended): The voltage regulator as set forth in Claim 3 wherein the source/drain circuit of said PMOS field-effect transistor (10) is selected ~~so~~

sufficiently wide that said voltage regulator can operate as a low-dropout voltage regulator.

Claim 5 (currently amended): The voltage regulator as set forth in Claim 4 2 wherein said transistor (10) is a PNP transistor.

Claim 6 (currently amended): A voltage regulator including a transistor (10), having a main current path between the input voltage terminal (V_{in}) of said voltage regulator and the output of said voltage regulator, comprising:

an amplifier (20) having an output being connected to the control terminal (16) of said transistor (10) and to the one input (22) of which a voltage as a function of the output voltage (V_{out}) of said voltage regulator is applied,

a transconductance amplifier (30) having a output being connected to the other input (24) of said amplifier (20),

a first resistor (R_{o1}),

a capacitor (C_c) wherein the one input (32) of said transconductance amplifier (30) is connected to a further voltage as a function of said output voltage (V_{out}) of said voltage regulator whilst the other input (34) of said transconductance amplifier (30) is connected to a reference voltage (V_{ref}) dictating said output voltage (V_{out}) of said voltage regulator, and

a further resistor (R_{sz}) is coupled between the one input (22) and the other input (24) of said amplifier (20),

~~The voltage regulator as set forth in Claim 1~~ wherein the value of said capacitor (C_c) is selected so that as of a critical value of a current flowing at the output of said voltage regulator the cutoff frequency of said transconductance amplifier (30) is lower than that of said amplifier (20).

Claim 7 (currently amended): A voltage regulator including a transistor (10), having a main current path between the input voltage terminal (V_{in}) of said voltage regulator and the output of said voltage regulator, comprising:

an amplifier (20) having an output being connected to the control terminal (16) of said transistor (10) and to the one input (22) of which a voltage as a function of the output voltage (V_{out}) of said voltage regulator is applied,

a transconductance amplifier (30) having a output being connected to the other input (24) of said amplifier (20),

a first resistor (R_{o1}),

a capacitor (C_c) wherein the one input (32) of said transconductance amplifier (30) is connected to a further voltage as a function of said output voltage (V_{out}) of said voltage regulator whilst the other input (34) of said transconductance amplifier (30) is connected to a reference voltage (V_{ref}) dictating said output voltage (V_{out}) of said voltage regulator, and

a further resistor (R_{sz}) is coupled between the one input (22) and the other input (24) of said amplifier (20),

~~The voltage regulator as set forth in Claim 1~~ wherein the value of said first resistor (R_{o1}) is adapted to the transconductance of said error amplifier (30).

Claim 8 (currently amended): The voltage regulator as in Claim 4 6 wherein said voltage regulator is configured as a monolithic integrated semiconductor circuit.